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(54) MULTI-PIECE CELL, AND MAGNETIC RANDOM ACCESS MEMORY ARRAY INCLUDING THE CELL

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a new memory cell structure and a memory array structure used for a MRAM device that can achieve a low power consumption of word current.
SOLUTION: The new type memory cell structure 20 for a magnetic random access memory has many partial cell pieces 21-24, and digital information is stored in the partial cell pieces 21-24. Each of partial cell piece 21-24 is formed by magnetic layers 27, 28 separated by conduction layers 29. A word line 25 is positioned near each partial cell piece so that it winds around partial cell pieces and winds on the same surface as partial cell pieces. Thereby, a low power consumption is achieved and word current is effectively utilized.

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CLAIMS

[Claim(s)]

[Claim 1] It is a magnetic random access memory cell (20 40), and is the cel piece (21-24) of :plurality. The cel piece which has two or more magnetic layers estranged by the conductive layer; in order to impress the magnetic field generated according to the WORD current which is a WORD line (25 41) and flows on the WORD line concerned to said cel piece In order to detect the condition of being WORD line; and the sense line (26) which are positioned near a cel piece, and having been saved at said memory cell The magnetic random access memory cell characterized by consisting of sense line; by which series connection is electrically carried out to said cel piece.

[Claim 2] It is a memory array in a magnetic random-access memory device (50), and they are two or more memory cells (56-60) arranged in on vertical Rhine and horizontal Rhine in the shape of a :matrix. each memory cell concerned — the 1- having a cel piece to the Nth, each cel piece concerned has two or more magnetic layers estranged by the conductive layer -- The memory cell of a place; so that it is two or more WORD lines (WO-WN), and a certain WORD line may be equivalent to each vertical Rhine and the magnetic field generated according to the WORD current which flows on the WORD line concerned may be impressed to

said cel piece Said each WORD line is positioned near [said / each] the cel piece of each memory cell in the shape of [said] vertical Rhine. The memory array which are WORD line [of a place];, and two or more sense lines (SO-SM), and is characterized by consisting of sense line; by which series connection is electrically carried out to said cel piece in order to detect the condition of being saved at said memory cell.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] Generally especially this invention relates to the memory cell structure of magnetic random access memory about magnetic random access memory.
[0002]
[Description of the Prior Art] Magnetic (magnetic) random access memory (MRAM) consists of two or more memory cells which align at a WORD line (word line) and a sense line (sense line), and, typically, each memory cell has two magnetic layers estranged by a conductive layer or the insulating layer. The structure of MRAM is the application number 08 which is coincidence connection U.S. application / 933, name "FERROMAGNETIC GMR MATERIAL AND METHOD OF FORMING AND USING" (filing date of application 6.6.1995) and the application number 08 that is coincidence connection U.S. application / 136, and name "GMRMATERIAL AND METHOD OF FORMING AND USING" (indicated at filing date of application 6.6.1995.). [553 and 933] [554 and 136] They are incorporated as bibliography into this specification.
[0003] The perspective view of the typical magnetic-substance memory cell 10 used for MRAM is shown in drawing 1 . A memory cell 10 has the 1st magnetic layer 11 and the 2nd magnetic layer 12 which are estranged by the conductive layer 13. A magnetic-substance ingredient (for example, NiFeCo) is used for the 1st magnetic layer 11 and 12, and a conductive layer 13 uses copper (Cu) for it. The 3 layer 11, and 12 and 13 are doubled, and a huge magnetic-reluctance (a giant magneto-resistive (GMR)) ingredient (material) is formed. The WORD line 14 (the Ward current is conducted) is positioned near the 1st magnetic layer 11, and, thereby, supplies the magnetic field generated according to the Ward

current into a GMR ingredient. A sense line 15 (a sense current is conducted) connects with GMR in ohmic contact, and, thereby, detects magnetic reluctance.

[0004] Digital information is expressed as a direction of the magnetic vector in magnetic layers 11 and 12. The digital information maintains eternally the condition (state) of having been given until the information is intentionally changed by the non-opposed magnetic field exceeding a threshold level. In order to change or write in the condition of a memory cell 10, all the magnetic fields (the magnetic field is enough to switch the direction of the magnetic vector of magnetic layers 11 and 12) generated according to the Ward current and a sense current are impressed to a memory cell 10. In order to read the condition of a memory cell 10, the electrical potential difference on a sense line 15 is compared with reference voltage by the comparator (not shown), and output voltage is impressed as digital information saved at a memory cell.

[0005] When the electrical potential difference on a sense line 15 is compared with reference voltage, parallel lay length (L) of a ******** is very more desirable than vertical width of face (W) to the sense line 15 of magnetic layers 11 and 12 to the sense line 15 of magnetic layers 11 and 12. Since the ratio (L/W) (it is a bigger value than 5 typically) of bigger die-length opposite width of face is chosen, when a magnetic field is added to magnetic layers 11 and 12, higher cell resistance is brought to magnetic layers 11 and 12. Therefore, higher output voltage covers a memory cell 10, and may occur (appeared).

[0006] However, the still bigger current for the higher switching field (switching field) in the cel brought about by the larger L/W ratio is needed, so that the high cell resistance is needed. Generally, 50mA or the Ward current beyond it is supplied to a WORD line. This means that it is required in the condition of a memory cell that a magnetic field should be impressed with high current density [in / for read-out (reading) and writing (writing) / appropriately / a WORD line].

[0007] Furthermore, when the ratio (L/W) of higher die-length (L) opposite width of face (W) is chosen, other problems occur. The WORD line 14 has the almost same width of face as the die length (L) of the magnetic layers 11 and 12 of a direction in alignment with a sense line 15. Therefore, all the WORD currents that are the products (procuct) of the current density of a WORD line and the width of face of a WORD line increase.

[0008] Therefore, one of the purposes of this invention is new to the MRAM device which attains the low power consumption of the Ward current,

and it is offering the improved memory cell structure.
[0009] Other purposes of this invention are offering the memory cell [which is used for the MRAM device which uses the Ward current effectively] structure which was new and was improved.
[0010] Furthermore, the purpose of this invention is also offering the memory array [which is used for a MRAM device] structure which was new and was improved.
[0011]
[Detailed explanation of a suitable example] Drawing according to this invention which simplified the memory cell 20 and was expanded is illustrated by drawing 2 . A memory cell 20 is formed of four cel pieces 21-24, the WORD line 25, and a sense line 26. Although the memory cell 20 (formed on a semi-conductor substrate (not shown)) contains four pieces (pieces) in these examples, please understand that a memory cell 20 may consist of any cel pieces of one or more numbers. Each cel piece is formed of at least two magnetic layers 27 and 28 estranged by the conductive layer 29, respectively. The WORD line 25 is twisted around the cel pieces 21-24 one after another. A sense line 26 is electrically connected to the cel pieces 21-24 in succession by ohmic contact.
[0012] Each cel pieces 21-24 have die length (L) in the direction in alignment with a sense line 26, and have width of face (W) to the perpendicular direction of a sense line 26 in a list. The ratio R of the die length (L) to width of face (W) is larger than 1, and 1.25 is chosen from 5 as a small type target. Each cel pieces 21-24 have and estrange distance of a gap (G) from other cel pieces. Typically, a gap (G) is equal to width of face (W).
[0013] The magnetic vector of the magnetic layers 27 and 28 of the cel piece 21 is oriented in the direction along the magnetic field generated according to the Ward current in the WORD line 25. The turn (rotate) of a magnetic vector is easily attained, so that said ratio R approaches 1. That is, although the condition of the cel piece 21 is switched, only the smaller Ward current is needed. However, as the resistance covering magnetic layers 27 and 28 falls, the output voltage generated in a sense line 26 declines.
[0014] In order to mitigate this problem, this invention divides one memory cell into four cel pieces 21-24, and connects them continuously through a sense line 26. By it, though the Ward current maintains the amount of the same currents, the total resistance concerned continues and increases to the cel pieces 21-24 by one side.
[0015] The graph 31 illustrating the resistance or the voltage output of a memory cell 20 (drawing 2) to the magnetic field or all the magnetic

fields which are impressed is shown in drawing 3 . The axis of abscissa shows the reinforcement of the direction of either of the direction of a magnetic field and reinforcement (supports), i.e., the forward direction of the magnetic vector of a cel 20, or hard flow (opposes). Usually, it expresses with the voltage output of a cel 20. A curve 32 shows the magnetic-reluctance property (magnetoresistance characteristic) over various magnetic field strength corresponding to the one direction of a magnetic vector through a voltage output. A curve 33 indicates the magnetic-reluctance property corresponding to the same magnetic field strength to an opposite direction to be said one direction of a magnetic vector through a voltage output. In the right-hand side of 0, curves 32 and 33 showed the output voltage corresponding to the magnetic field of the direction which supports the vector of a curve 32, i.e., the direction which moves against the vector of a curve 33, and the magnetic field to the left-hand side of 0 is a direction which supports the vector of a curve 33, namely, they have turned to it in the direction which moves against the vector of a curve 32. Typically, curves 32 and 33 intersect an electrical-potential-difference shaft in the same point, and show the same minimum value. For explanation, a curve 33 shifts only a few perpendicularly and shows the difference between the curve.

[0016] The voltage output (V0) of a cel 20 is not concerned in the direction of a magnetic vector, but is almost the same in the magnetic field where 0 is impressed. A curve 33 shows the voltage output of a cel 20 which has the vector oriented with hard flow by all magnetic fields, and a curve 32 shows the voltage output of a cel 20 which has the vector oriented in the forward direction by all magnetic fields as the magnetic field increases to H1 from 0. In magnetic field strength H1, the vector in a memory cell 20 converts and shows output voltage V1. Orientation continues and the magnetic vector of a memory cell 20 changes in other directions near the magnetic field strength of H2 as total magnetic field strength increases between H1 and H2. In the H2 neighborhood, the vector of a memory cell 20 changes to hard flow, and the resistance corresponds to the value of H2, and the value beyond it, and falls. The output voltage corresponding to all the magnetic fields of hard flow in the same thing is shown also fromH3 to 0 and H4.

[0017] Drawing according to this invention which simplified other memory cells 20 and was expanded is illustrated by drawing 4 . The component of drawing 4 which has the same reference number as drawing 2 is the same or equivalent to the component with which drawing 2 corresponds. A memory cell 40 has the same structure as the memory cell 20 of drawing 2 except for the WORD line 41. A memory cell 40 is formed of four cel

pieces 21-24, the WORD line 41, and a sense line 26. Each cel piece is positioned in the distance of the same spacing. The WORD line 41 has wound on the cel pieces 21-24, and is formed on the same flat surface. A sense line 26 follows the cel pieces 21-24, continues and intersects a list on each cel section Kataue's WORD line 41, and is electrically connected by ohmic contact. A memory cell 40 has the same property as the property of the memory cell 20 shown in drawing 3 . A memory cell 40 may be simply manufactured easily rather than a memory cell 20. It is because the WORD line 41 is formed on the same flat surface.

[0018] The memory array 50 according to this invention which has a memory cell is shown in drawing 5 . Two or more memory cells are positioned in a memory array 50 by the array on the intersection part which WORD line WO-WN superimposes on sense lines SO-SM. WORD line WO-WN and sense lines SO-SM access a memory cell, in order to connect with an address decoder 51 and to change into read-out and the condition of writing by it. For example, memory cells 52-55 are positioned on the intersection part of WORD line WO-WN and sense lines SO-SM. two magnetic layers 27 and 28 by which a memory cell 52 has the 1st, 2nd, 3rd, and 4th cel pieces 56-59, and each cel piece is estranged by the conductive layer 29 — since — it is constituted and is the same structure as the cel piece 21 (drawing 2 , 4). Each memory cells 53-55 also have the 1st, 2nd, 3rd, and 4th cel pieces.

[0019] The WORD line WO is first positioned in the top-face side (top) of each 1st cel piece 56 of memory cells 52-55, and 60 grades, next returns the base side (bottom) of the 1st cel piece 56 and 60 grades. Then, the WORD line WO covers the 2nd cel piece bottom of each cel, and is bent. Such wiring is given to the 2nd, 3rd, and 4th cel pieces 57-59 as a WORD line WO. However, the WORD line WO can wire the base side of the 2nd cel piece 57 in memory cells 53-56 at the beginning, and then can also wire the top-face side of the 2nd cel piece 57. The WORD line WO winds the perimeter of each group of the 1st, 2nd, 3rd, and 4th cel pieces 56-59 continuously. Similarly, WORD line WO-WN also winds the perimeter of each group of a cel piece.

[0020] Thus, the memory cell more effective than the conventional memory cell was indicated. This new memory cell can be divided into two or more memory cells, in order that fewer Ward currents may read the condition of a memory cell or may write in by it, it is applied, and that Ward current is effectively used, in order to generate a magnetic field. Furthermore, the new memory array structure used for a memory cell is indicated. By the MRAM device adopted as the memory array, power consumption is reduced dramatically.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] Drawing which simplified the MRAM cel which has some GMR ingredients.

[Drawing 2] Drawing which simplified and expanded the MRAM cel according to this invention.

[Drawing 3] Drawing which made the graph the property of the GMR ingredient illustrated by drawing 2 .

[Drawing 4] Drawing which simplified and expanded other MRAM cels according to this invention.

[Drawing 5] Drawing having shown the memory array according to this invention which has a memory cell.

[Description of Notations]

10, 20, 40, and 52- 56 and 60 Magnetic-substance memory cell
11, 12, 27, 28 Magnetic layer
12 Magnetic Layer
13 29 Conductive layer
14, 25, 41 WORD line
15 26 Sense line
21, 22, 23, 24, 56-59 Cel piece
50 Memory Array
51 Address Decoder
WO-WN WORD line
SO-SM Sense line

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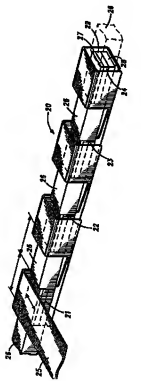
最終頁に続く

(54)【発明の名称】　マルチビースセルおよびそのセルを含む磁気ランダムアクセスメモリアレイ

(57)【要約】

【課題】　ワード電流の低電力消費を達成するMRAMデバイスに使用される新規なメモリセル構造、メモリアレイ構造を提供する。

【解決手段】　磁気ランダムアクセスメモリのための新しい型のメモリセル構造（２０、４０）を提供する。メモリセル（２０、４０）が、多数のセル部片（２１～２４）を有し、そのセル部片には、デジタル情報が保存される。各セル部片は導電層（２９）によって離間される磁性体層（２７、２８）によって形成される。ワードライン（２５、４１）が、セル部片（２１～２４）の周囲を曲がりくねり、セル部片（２１～２４）上の同一面上に曲がりくねるように、各セル部片付近に位置付けられる。本発明は、低消費電力を達成し、ワード電流を効果的に利用する。



【特許請求の範囲】

【請求項１】　磁気ランダムアクセスメモリセル（２０、４０）であって：複数のセル部片（２１～２４）であって、導電層によって離間される複数の磁性体層を有するセル部片；ワードライン（２５、４１）であって、当該ワードラインに流れるワード電流によって発生する磁場を前記セル部片に印加するために、セル部片の付近に位置付けられるワードライン；およびセンスライン（２６）であって、前記メモリセルに保存された状態を検知するために、前記セル部片に電気的に直列接続されるところのセンスライン；から構成されることを特徴とする磁気ランダムアクセスメモリセル。

【請求項２】　磁気ランダムアクセスメモリデバイス（５０）内にあるメモリアレイであって：マトリックス状に縦ラインおよび横ライン上に並べられる複数のメモリセル（５６～６０）であって、当該各メモリセルは第１～第Nまでのセル部片を有し、当該各セル部片は導電層によって離間される複数の磁性体層を有する、ところのメモリセル；複数のワードライン（W_0～W_N）であって、あるワードラインが各縦ラインに対応し、当該ワードラインに流れるワード電流によって発生する磁場を前記セル部片に印加するように、前記各ワードラインが各メモリセルの前記各セル部片付近に前記縦ライン状に位置付けられる、ところのワードライン；および複数のセンスライン（S_0～S_M）であって、前記メモリセルに保存されている状態を検知するために、前記セル部片に電気的に直列接続されているところのセンスライン；から構成されることを特徴とするメモリアレイ。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は一般に磁気ランダムアクセスメモリに関し、特に磁気ランダムアクセスメモリのメモリセル構造に関する。

【０００２】

【従来の技術および発明が解決しようとする課題】磁気（magnetic）ランダムアクセスメモリ（MRAM）が、ワードライン（word line）およびセンスライン（sense line）に整列する複数のメモリセルから成り、典型的には、各メモリセルは、導電層または絶縁層により離間せられる２つの磁性体層を有する。MRAMの構造は、同時係属米国出願である出願番号08/553,933,名称"FERROMAGNETIC GMR MATERIAL AND METHOD OF FORMING AND USING"（出願日6.6.1995）、および同時係属米国出願である出願番号08/554,136,名称"GMRMATERIAL AND METHOD OF FORMING AND USING"（出願日6.6.1995、に開示されている。それらは、本明細書中に参考文献として組み入れられている。

【０００３】図１には、MRAMに使用される典型的な磁性体メモリセル１０の斜視図が示されている。メモリセル１０は、導電層１３によって離間される第１磁性体層１１および第２磁性体層１２を有する。第１磁性体層１１、１２には、磁性体材料（例えばNiFeCo）を利用し、導電層１３は、例えば銅（Cu）を利用する。その３層１１、１２および１３を合わせて、巨大磁気抵抗（a giant magneto-resistive(GMR)）材料（material）が形成される。ワードライン１４（ワード電流を伝導する）が、第１磁性体層１１の近くに位置付けられ、それにより、GMR材料にワード電流によって発生する磁場を供給する。センスライン１５（センス電流を伝導する）が、GMRにオーミックコンタクトにて接続し、それにより磁気抵抗を検知する。

【０００４】デジタル情報が、磁性体層１１、１２における磁性ベクトルの方向として表される。そのデジタル情報は、その情報がしきい値レベルを超える不反対の磁場によって故意に変更せられるまでは、与えられた状態（state）を永久に維持する。メモリセル１０の状態を変更し、または書き込むために、ワード電流およびセンス電流によって発生する全磁場（その磁場は、磁性体層１１、１２の磁気ベクトルの方向を切り換えるのに充分である）が、メモリセル１０に印加される。メモリセル１０の状態を読むために、センスライン１５上の電圧がコンパレータ（図示せず）によって基準電圧と比較され、出力電圧が、メモリセルに保存されるデジタル情報として印加される。

【０００５】センスライン１５上の電圧が基準電圧と比較される場合、磁性体層１１、１２のセンスライン１５に対して平行方向の長さ（L）が、磁性体層１１、１２のセンスライン１５に対して垂直方向の幅（W）よりも非常に長いことが望ましい。より大きさ長さ対幅の比（L/W）（典型的には、５よりも大きな値である）が、選択されるので、磁場が磁性体層１１、１２に加えられるとき、磁性体層１１、１２には、より高いセル抵抗がもたらされる。従って、より高い出力電圧が、メモリセル１０に亘って発生し（appeared）得る。

【０００６】しかしながら、高いそのセル抵抗が必要とされる程、より大きいL/W比によってもたらされるセルにおける、より高いスイッチング領域（switching field）のために、ますます大きな電流が必要とされる。一般に、例えば、50mAまたはそれ以上のワード電流が、ワードラインに供給される。このことは、メモリセルの状態を適切に読出し（reading）および書込み（writing）のために、ワードラインにおける高い電流密度により、磁場が印加されることが要求されることを意味する。

【０００７】さらに、より高い長さ（L）対幅（W）の比率（L/W）が選択される場合、他の問題が発生する。ワードライン１４は、センスライン１５に沿った方向の磁性体層１１、１２の長さ（L）とほぼ同じ幅を有する。従って、ワードラインの電流密度およびワードラインの幅の所産（procuct）である全ワード電流が、増加する。

【０００８】故に、本発明の目的の１つは、ワード電流の低電力消費を達成するMRAMデバイスに、新しく、また改良されたメモリセル構造を提供することである。

【０００９】本発明の他の目的は、効果的にワード電流を利用するMRAMデバイスに使用される新しく、また改良されたメモリセル構造を提供することである。

【００１０】さらに本発明の目的は、MRAMデバイスに使用される新しく、また改良されたメモリアレイ構造を提供することでもある。

【００１１】

【好適実施例の詳細な説明】図２には、本発明に従った、メモリセル２０を単純化し、拡大した図が図示されている。メモリセル２０は、４個のセル部片２１～２４、ワードライン２５およびセンスライン２６により形成される。メモリセル２０（半導体基板（図示せず）上に形成される）は、これらの実施例においては４個の部片（pieces）を含んでいるが、メモリセル２０は、１個以上のいずれの数のセル部片からも構成され得ることを理解されたい。各セル部片は、それぞれ導電層２９によって離間される少なくとも２個の磁性体層２７、２８によって形成される。ワードライン２５は、セル部片２１～２４に次々に巻き付けられる。センスライン２６は、セル部片２１～２４にオーミックコンタクトによって、連続して電気的に接続される。

【００１２】各セル部片２１～２４は、センスライン２６に沿った方向に長さ（L）、並びにセンスライン２６の垂直方向に幅（W）を有する。幅（W）に対する長さ（L）の比率Rは、1よりも大きく、5よりも小さい、典型的には1.25が選択される。各セル部片２１～２４は、他のセル部片からギャップ（G）の隔たりをもって離間する。典型的には、ギャップ（G）は幅（W）に等しい。

【００１３】セル部片２１の磁性体層２７、２８の磁気ベクトルは、ワードライン２５におけるワード電流によって発生する磁場に沿った方向に方向付けられる。前記比率Rが1に近づくほど、磁気ベクトルは容易に転向（rotate）可能になる。即ち、セル部片２１の状態を切り換えるのに、より小さなワード電流しか必要とされない。しかしながら、磁性体層２７、２８に亘る抵抗が低下するのと同様に、センスライン２６に発生する出力電圧が低下する。

【００１４】この問題を軽減するために、本発明は１個のメモリセルを４個のセル部片２１～２４に分割し、センスライン２６を介してそれらを連続的に接続する。それによって、ワード電流が同一電流量を維持しながらも、一方で当該全抵抗は、セル部片２１～２４に亘って増加する。

【００１５】図３には、印加される磁場または全磁場に対するメモリセル２０（図２）の抵抗または電圧出力を図示するグラフ３１が示される。その横軸は、磁場方向および強度、即ち、セル２０の磁気ベクトルの正方向（supports）または逆方向（opposes）のどちらかの方向の強度を示す。通常、セル２０の電圧出力で表す。曲線３２が、電圧出力を介し磁気ベクトルの一方向に対応する様々な磁場強度に対する、磁気抵抗特性（magneto resistance characteristic）を示す。曲線３３が、磁気ベクトルの前記一方向とは反対の方向への同様な磁場強度に対応する磁気抵抗特性を、電圧出力を介して示す。0の右側においては、曲線３２、３３は、曲線３２のベクトルを支持する方向、即ち曲線３３のベクトルに逆行する方向の磁場に対応する出力電圧を示し、0の左側への磁場は、曲線３３のベクトルを支持する方向であり、即ち曲線３２のベクトルに逆行する方向に向いている。典型的に、曲線３２、３３は、同一点において電圧軸と交差し、同一最小値を示す。説明のため、曲線３３は、垂直方向に少しだけずらし、その曲線間の違いを示している。

【００１６】0が印加される磁場では、セル２０の電圧出力（V_0）が、磁気ベクトルの方向に関わらず、ほぼ同一である。その磁場が、0からH_1へ増加するに従い、曲線３３は、全磁場によって逆方向に方向付けられるベクトルを有するセル２０の電圧出力を示し、曲線３２は、全磁場によって正方向に方向付けられるベクトルを有するセル２０の電圧出力を示す。磁場強度H_1においては、メモリセル２０内のベクトルは、転向し、出力電圧V_1を示す。全磁場強度がH_1とH_2との間において増加するに従い、メモリセル２０の磁気ベクトルは、方向付けが続き、H_2の磁場強度付近での他の方向に切り替わる。H_2付近では、メモリセル２０のベクトルは逆方向に切り替わり、その抵抗は、H_2の値およびそれ以上の値に対応し、低下する。同様なことが、逆方向の全磁場に対応する出力電圧が、0とH_3からH_4との間にも示される。

【００１７】図４には、本発明に従った、他のメモリセル２０を単純化し、拡大した図が図示されている。図２と同じ参照番号を有する図４の構成要素は、図２の対応する構成要素と同一または同等である。メモリセル４０が、ワードライン４１を除いて、図２のメモリセル２０と同じ構造を有する。メモリセル４０は、４個のセル部片２１～２４、ワードライン４１およびセンスライン２６により形成される。各セル部片は、同一の間隔の距離で位置付けられている。ワードライン４１は、セル部片２１～２４の上に曲がりくねっており、同一平面上に形成される。センスライン２６は、セル部片２１～２４に連続して、並びに各セル部片上のワードライン４１に亘って交差し、電気的にオーミックコンタクトにより接続される。メモリセル４０は、図３に示されるメモリセル２０の特性と同一の特性を有する。メモリセル４０は、メモリセル２０よりも簡単に、容易に製造され得る。ワードライン４１が同一平面上に形成されるからである。

【００１８】図５には、本発明に従った、メモリセルを有するメモリアレイ５０を示す。メモリアレイ５０にお

いては、ワードラインW_0～W_NがセンスラインS_0～S_Mと重畳する交差部分上のアレイに、複数のメモリセルが位置付けられる。ワードラインW_0～W_NおよびセンスラインS_0～S_Mは、アドレスデコーダ５１に接続し、それによって、読出し、および書込みの状態にするために、メモリセルにアクセスする。例えば、メモリセル５２～５５が、ワードラインW_0～W_NとセンスラインS_0～S_Mとの交差部分上に位置付けられる。メモリセル５２は、第１、第２、第３および第４のセル部片５６～５９を有し、各セル部片は、導電層２９によって離間される２つの磁性体層２７、２８をから構成され、セル部片２１（図２、４）と同一の構造である。各メモリセル５３～５５も、第１、第２、第３および第４のセル部片を有する。

【００１９】ワードラインW_0は、メモリセル５２～５５の各第１セル部片５６、６０等の上面側（top）に最初に位置付けられ、次に、第１セル部片５６、６０等の底面側（bottom）を戻ってくる。その後、ワードラインW_0は、各セルの第２セル部片の上側に亘って曲げられる。このような配線は、ワードラインW_0として、第２、第３および第４のセル部片５７～５９に施される。しかし、ワードラインW_0は、最初にメモリセル５３～５６における第２セル部片５７の底面側に配線し、次に第２セル部片５７の上面側に配線することもできる。ワードラインW_0は、第１、第２、第３および第４のセル部片５６～５９の各グループの周囲を連続して曲がりくねる。同様にして、ワードラインW_0～W_Nも、セル部片の各グループの周囲を曲がりくねる。

【００２０】このように、従来のメモリセルよりも効果的なメモリセルが開示された。この新規なメモリセルは、複数のメモリセルに分割でき、それによって、より少ないワード電流が、メモリセルの状態を読み出したり、書き込むために適用され、そのワード電流は磁場を発生させるために、効果的に使用される。さらに、メモリセルに利用される新規なメモリアレイ構造が、開示されている。そのメモリアレイに採用されるMRAMデバイスによって、電力消費が劇的に削減される。

【図面の簡単な説明】

【図１】GMR材料の一部分を有するMRAMセルを簡単化した図。

【図２】本発明に従った、MRAMセルを簡単化し、拡大した図。

【図３】図２に図示されるGMR材料の特性をグラフにした図。

【図４】本発明に従った、他のMRAMセルを簡単化し、拡大した図。

【図５】本発明に従った、メモリセルを有するメモリアレイを示した図。

【符号の説明】

１０、２０、４０、５２～５６、６０　磁性体メモリセル

１１、１２、２７、２８　磁性体層

１２　磁性体層

１３、２９　導電層

１４、２５、４１　ワードライン

１５、２６　センスライン

２１、２２、２３、２４、５６～５９　セル部片

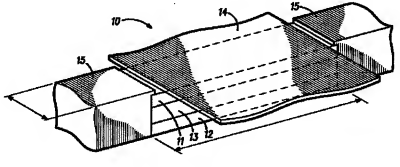
５０　メモリアレイ

５１　アドレスデコーダ

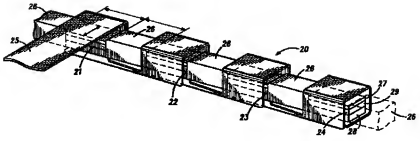
W_0～W_N　ワードライン

S_0～S_M　センスライン

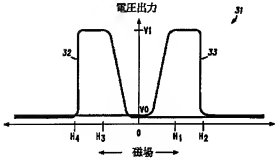
【図１】



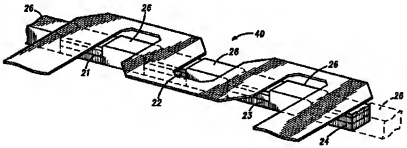
【図2】


25
21
22
23
24
26
27
28
29
20

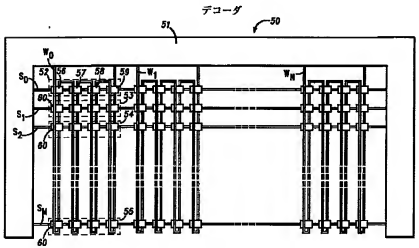
【図3】


電圧出力
31
V1
V0
32
33
H4
H3
0
H1
H2
磁場

【図4】


26
21
22
23
24
40

【図5】


デコーダ
50
51
W0
W1
WN
S0
S1
S2
SN
52
56
57
58
59
60
53
54
55

フロントページの続き

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【外国語明細書】

A MULTI-PIECE CELL AND A MRAM ARRAY INCLUDING THE CELL

Field of the Invention

The present invention relates to a magnetic random access memory, and more particularly, to a memory cell structure of a magnetic random access memory.

Background of the Invention

A magnetic random access memory (MRAM) consists of a plurality of memory cells arrayed on intersections of word lines and sense lines, each memory cell typically having two magnetic layers separated by a conductive or insulating layer. Structures of MRAMs are disclosed in copending applications bearing serial number 08/553,933, titled "FERROMAGNETIC GMR MATERIAL AND METHOD OF FORMING AND USING", filed June 6, 1995, and bearing serial number 08/554,136, titled "GMR MATERIAL AND METHOD OF FORMING AND USING", filed June 6, 1995, which are hereby incorporated by reference herein.

FIG. 1 shows a perspective view of a typical magnetic memory cell 10 used in the MRAM. Memory cell 10 has a first magnetic layer 11 and a second magnetic layer 12 separated by a conductive layer 13. Layers 11 and 12 utilize magnetic material such as NiFeCo, and conductive layer 13 utilizes, for example, Copper (Cu). The three layers 11, 12, and 13 together form a giant magneto-resistive (GMR) material. A word line 14, which carries a word current, is placed adjacent first layer 11 in order to provide the GMR material with a magnetic field generated by the word curre

nt. A sense line 15, which carries a sense current, is connected to the GMR with an ohmic contact to sense a magnetic resistance.

Digital information is represented as a direction of magnetic vectors in magnetic layers 11 and 12, and the information indefinitely remains in a given state until the information is intentionally changed by an opposite magnetic field over a threshold level. In order to write or change a state in memory cell 10, a total magnetic field generated by the word current and the sense current is applied to memory cell 10 that is sufficient to switch the direction of the magnetic vectors in magnetic layers 11 and 12. To read the state in memory cell 10, a voltage on sense line 15 is compared with a reference voltage by a comparator (not shown) and an output voltage is provided as a digital information stored in the memory cell.

When the voltage on sense line 15 is compared with the reference voltage, it is desirable that a length (L) along sense line 15 of magnetic layers 11 and 12 is much longer than a width (W) of layers 11 and 12 perpendicular to sense line 15. Because the greater a ratio (L/W) of the length to the width, typically a value more than five, is selected, the higher a cell resistance is appeared in magnetic layers 11 and 12 when a magnetic field is applied to the layers. Accordingly, the higher output voltage can be appeared over the memory cell 10.

However, the higher the cell resistance needed, the more current is required to operate due to the higher switching field of the cell caused by a larger L/W ratio. Generally, a 50 mA or more word current, for example, is applied in the word line. This means that a high current density in the word line is required to apply the magnetic field for appropriately reading and writing a state in the memory cell.

Furthermore, another problem arises when the higher ratio (L/W) of the length (L) to the width (W) is selected. Word line 14 has almost the same

width as the length (L) of magnetic layers 11 and 12 along sense line 1
5. Accordingly, a total word current, which is a product of the width o
f the word line and the current density in the word line, increases.

Therefore, it is a purpose of the present invention to provide a new and
improved memory cell structure used in a MRAM device which attains a lo
w power consumption of the word current.

It is another purpose of the present invention to provide a new and impr
oved memory cell structure used in a MRAM device which effectively utili
zes the word current.

It is still another purpose of the present invention to provide a new an
d improved memory array structure used in a MRAM device.

Summary of the Invention

This need and others are substantially met through provision of a MRAM c
ell which has a plurality of cell pieces, a word line and a sense line.
Each cell piece, which is formed by magnetic layers separated by a cond
uctor layer, is connected in series with each other piece by the sense l
ine. The word line is placed adjacent magnetic layers of each cell piec
e where the sense line is crossed over.

Brief Description of the Drawings

FIG. 1 shows a simplified MRAM cell having a portion of GMR material.

FIG. 2 shows a simplified and enlarged memory cell in accordance with th
e present invention.

FIG. 3 shows a graph illustrating characteristics of the GMR material sh
own in FIG. 2.

FIG. 4 shows another simplified and enlarged memory cell in accordance w

ith the present invention.

FIG. 5 shows a memory array having memory cells in accordance with the p resent invention.

Detailed Description of the Preferred Embodiments

FIG. 2 shows a simplified and enlarged memory cell 20 in accordance with the present invention. Memory cell 20 is formed by four cell pieces 21 -24, a word line 25, and a sense line 26. While memory cell 20, which i s formed on a semiconductor substrate (not shown), includes four pieces in these examples it should be understood that memory cell 20 may be com prised of any number of cell pieces greater than one. Each cell piece i s made up by at least two magnetic layers 27 and 28 separated by a condu ctor layer 29, respectively. Word line 25 is wound around cell pieces 2 1-24 one after another. Sense line 26 is electrically connected in seri es to cell pieces 21-24 with ohmic contacts.

Each cell piece 21-24 has a length (L) along sense line 26 and a width (W) perpendicular to sense line 26. A ratio R of the length (L) to the w idth (W) is greater than 1 and less than 5, and typically 1.25 is select ed. Each cell piece 21-24 is placed a gap (G) apart from another cell p iece, which gap (G) is typically equal to the width (W).

Magnetic vectors in magnetic layers 27 and 28 of cell piece 21 are orien ted along a magnetic field generated by a word current in word line 25. The closer to 1 the ratio R is, the easier the magnetic vectors can rot ate, that is, less word current is needed to switch a state in cell piec e 21. An output voltage appearing on sense line 26, however, decreases as well because the resistance over magnetic layers 27 and 28 decreases. To reduce this issue, this invention divides one memory cell to four cel l pieces 21-24 and serially couples them via sense line 26, thereby the

total resistance increases over cell pieces 21-24, while maintaining the same amount of the word current.

FIG. 3 shows a graph 31 illustrating the resistance or voltage output of memory cell 20 (FIG. 2) verses the applied magnetic field or total magnetic field. The abscissa indicates magnetic field direction and strength, that is, the strength either supports or opposes the magnetic vectors of cell 20. The ordinate represents the voltage output of cell 20. A curve 32 indicates the magnetoresistance characteristic, via the output voltage, for various magnetic field intensities for one direction of magnetization vectors. A curve 33 indicates the magnetoresistance characteristic, via the output voltage, for the same magnetic field intensities for the opposite direction of magnetization vectors. To the right of zero, curves 32 and 33 indicate the output voltage for magnetic fields that support the vectors of curve 32 and oppose the vectors of curve 33, and magnetic fields to the left of zero support the vectors of curve 33 and oppose the vectors of curve 32. Typically, curves 32 and 33 cross the voltage axis at the same point and have the same minimum values. For the sake of explanation, curve 33 is shifted vertically a slight amount to show the differences between the curves.

At zero applied field, the voltage output (V0) of cell 20 is approximately the same regardless of the magnetization vector direction. As the field increases from zero to H1, curve 32 shows the voltage output of cell 20 having vectors that are opposed by the total magnetic field, and curve 32 shows the voltage of cell 20 having vectors that are supported by the magnetic field. At magnetic field intensity of H1, the vectors in memory cell 20 rotate and indicate the output voltage V1. As the total magnetic field intensity increases between H1 and H2, the magnetic vectors of memory cell 20 continue to rotate and snap to the other direction near a field intensity of H2. Near H2, the vectors of memory cell 20 sna

p to the opposite direction and the resistance decreases for values of H 2 and above. Similarly, the output voltage for an opposite direction to tal magnetic field is shown between zero and H2 to H4.

FIG. 4 shows another simplified and enlarged memory cell 40 in accordanc e with the present invention. Elements of FIG. 4 that have the same ref erence numbers as FIG. 2 are the same or equivalent as the corresponding FIG. 2 elements. Memory cell 40 has the same structure as memory cell 20 in FIG. 2 except for a word line 41. Memory cell 40 is formed by fou r cell pieces 21-24, a word line 41, and sense line 26. Each cell piece is located at the same interval distances. Word line 41 is formed on t he same plane and meanders on top of cell pieces 21-24. Sense line 26 i s electrically connected with ohmic contacts to cell pieces 21-24 in ser ies and crosses over word line 41 on each cell piece. Memory cell 40 ha s the same characteristics shown in FIG. 3 as memory cell 20. Memory ce ll 40 can be produced more simply and easily than memory cell 20 because word line 41 is formed on the same place.

FIG. 5 shows a memory array 50 having memory cells in accordance with th e present invention. In memory array 50, a plurality of memory cells ar e disposed in an array on intersections where word lines W0-WN cross ove r sense lines S0-SM. Word lines W0-WN and sense lines S0-SM are connect ed to an address decoder 51 by which a memory cell is accessed for readi ng and writing a state. Memory cells 52-55, for example, are located on intersections of word line W0 and sense lines SN SM. Memory cell 52 ha s first, second, third, and fourth cell pieces 56-59, each cell piece co mprising two magnetic layers 27 and 28 separated by a conductor layer 29 , which is the same structure as cell piece 21 (FIGS 2 and 4). Each mem ory cell 53-55 has first, second, third, and fourth cell pieces as well. Word line W0 is positioned first on the top of each first cell piece 56, 60, etc. in memory cells 52-55, then returns on the bottom of first cel

l pieces 56. 60, etc. after which it winds over to the tops of the secon d cell pieces of each of the cells. This wiring is carried out to secon d, third, and fourth cell pieces 57-59 for word line W0. However, word line W0 may be wired first on the back of second cell piece 57 in memory cells 53-56, then on the top of second cell piece 57. Word line W0 is wound in series around each group of first, second, third, and fourth ce ll pieces 56-59. In a similar fashion, word lines W1-WN are also wound around each group of cell pieces.

Thus, a memory cell which is more efficient than prior memory cell is di sclosed. The novel memory cell is divided into a plurality of cell piec es, thereby less amount of a word curren: can be applied to read and wri te a state in the memory cell and the word current is efficiently used f or generating a magnetic field. Furthermore, a novel memory array struc ture utilizing the memory cell is explained. The MRAM device employing the memory array allows the power consumption to be dramatically reduced .

CLAIMS

1. A magnetic random access memory cell (20. 40) comprising:

a plurality of cell pieces (21-24), each cell piece having a plurality o f magnetic layers separated by.a conductor layer;

a word line (25, 41), placed adjacent the cell pieces. for applying a ma gnetic field created by a word current flowing in the word line to the c ell pieces; and

a sense line (26), electrically connected to the cell pieces in series f or sensing a state stored in the memory cell.

2. A memory array in a magnetic random access memory device (50) co

mprising:

a plurality of memory cells (S6-60) arrayed on row lines and columu line s in a matrix, each memory cell having first to Nth cell pieces, each ce ll piece having a plurality of magnetic layers separated by a conductor layer;

a plurality of word lines (W0-WN), one word line for each column line, e ach word line placed adjacent each of the cell pieces of each memory cel l in the column line, for applying a magnetic field created by a word cu rrent flowing in the word line to the cell pieces; and

a plurality of sense lines (S0-SM), each sense line electrically connect ed to the cell pieces in series for sensing a state stored in the memory cell.

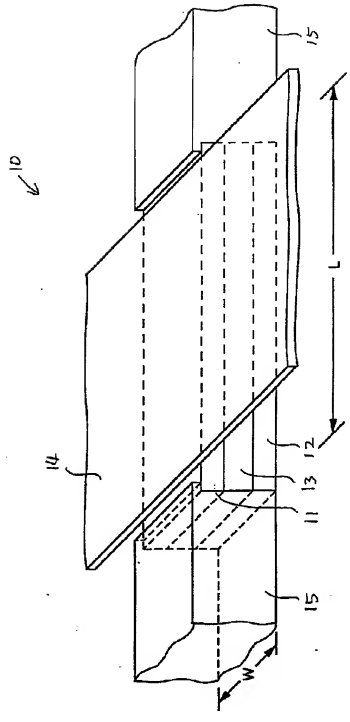


FIG. 1

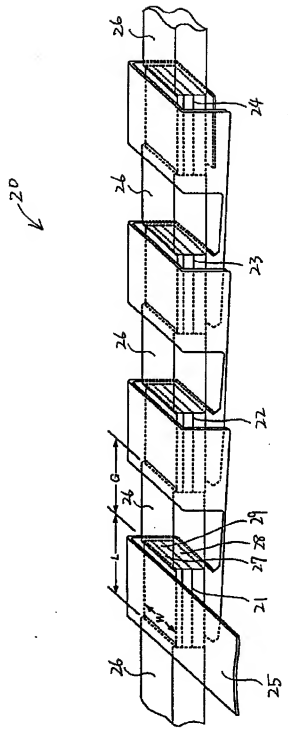
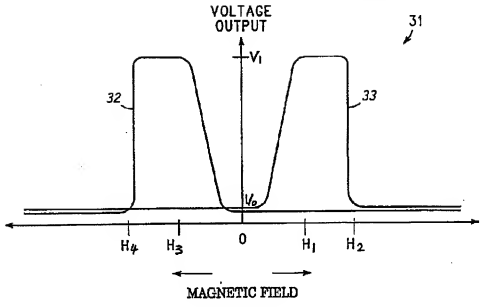


FIG. 2

FIG. 3



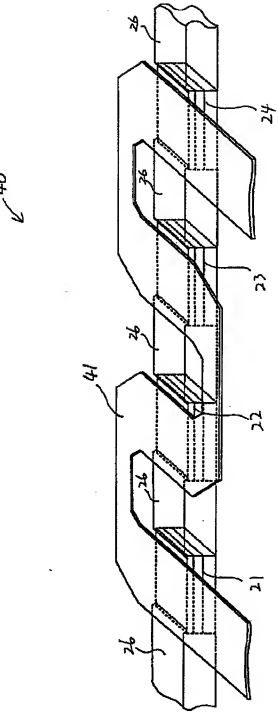


FIG. 4

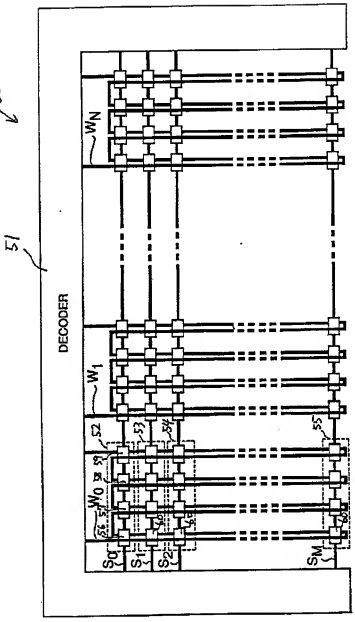


FIG. 5

Abstract of the Disclosure

New types of memory cell structures (20,40) for a magnetic random access memory are provided. A memory cell (20,40) has a plurality of cell pieces (21-24) where digital information is stored. Each cell piece is formed by magnetic layers (27,29) separated by a conductor layer (28). A word line (25,41) is placed adjacent each cell piece for winding around cell pieces (21-24) and meandering on a same plane on cell pieces (21-24), for example. The invention attains less power consumption and effective usage for a word current.